

CLAIMS

1. A digital VCO, comprising:
a quartz oscillation circuit generating a signal
5 having a predefined frequency by using a quartz oscillator;
a conversion circuit converting a given analog signal to a digital signal; and
a divider circuit dividing a frequency of signal
10 generated in said quartz oscillation circuit by a division ratio according to said digital signal.
2. The digital VCO in claim 1, further comprising
a sample holding circuit taking in a digital signal
15 outputted from said conversion circuit in a predefined interval.
3. The digital VCO in claim 2, wherein
said sample holding circuit, whose sampling time
is longer interval than that used by said conversion
20 circuit, holds and outputs a digital signal taken in from said conversion circuit within a holding time.
4. The digital VCO in claim 1, further comprising
a compensation circuit compensating for an offset
25 error of said digital signal occurring in said conversion

circuit.

5. The digital VCO in claim 1, further comprising
a limit circuit limiting a variation range of said
5 division ratio.

6. A PLL circuit adjusting a phase difference between
an input signal and a base signal, including:
a detection circuit detecting a phase difference
10 between said input signal and a base signal;
conversion means for converting a signal
indicating said phase difference to a digital signal;
a quartz oscillation circuit generating a signal
having a predefined frequency by using a quartz
15 oscillator; and
a divider circuit dividing a frequency of signal
generated by said quartz oscillation circuit by a
division ratio according to said digital signal, wherein
a phase difference between said input signal and
20 said base signal is adjusted according to a divided
frequency signal by said divider circuit.

7. The PLL circuit in claim 6, further comprising
a sample holding circuit taking in, in a predefined
25 interval, digital data outputted from said conversion

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circuit.